

**AMENDMENTS TO THE SPECIFICATION**

Please replace the first full paragraph on page 5 with the following:

Also, the configuration of Figure 1 shows a data signal line loading circuit 13 which includes the resistor R connected to the data signal line DL. The resistor R has a predetermined resistance such as 1K Ohms. The resistor R is also connected to the capacitor C1 and the source region of transistor Tr2. The capacitor C1 has a predetermined storage capacitance such as 5 pico farad.

Please replace the second full paragraph on page 5 with the following:

Figure 1 further shows the gate electrode of transistor Tr2, the gate electrode of transistor Tr3, and also the gate electrode of transistor Tr4 connected to scan line SCAN 2. The source region of transistor Tr3 is connected to power source VDD while the drain region of transistor Tr3 is connected to the source region of transistor Tr4 and is also connected to the drain region of transistor Tr2. Transistor Tr2 is a switching transistor and may be n-channel transistor or p-channel transistor.

Please replace the third full paragraph on page 5 with the following:

Figure 1 also shows a transistor Tr5, a transistor Tr6, an OLED D, a parasitic capacitor C2 and a storage capacitor C3. The OLED D has an anode and a cathode. The gate electrode of transistor Tr5 is connected to the storage capacitor C3 and the drain region of transistor Tr4. The transistor Tr4 is provided to initialize the stored voltage at the storage capacitor C3. Furthermore, the drain region of transistor Tr5 is

connected to the OLED D as well as the parasitic capacitor C2. The OLED D is connected to power source VSS at the opposite end.